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Application No.: 09/870,280

Docket No.: MWS-040RCE

**AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A computer implemented modeling process comprising:  
    providing a plurality of blocks, each of the blocks representing functional entities;  
    generating a plurality of output signal values from the plurality of blocks;  
    grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; ~~and~~  
    outputting the first composite signal; and  
    storing the first composite signal in a storage device.
2. (Previously Presented) The process of claim 1 wherein each of the blocks includes at least one output signal port.
3. (Previously Presented) The process of claim 1 wherein a plurality of input signal values and the output signal values have at least one attribute.
4. (Original) The process of claim 3 wherein the attribute is a name.
5. (Original) The process of claim 3 wherein the attribute is a data type.
6. (Original) The process of claim 3 wherein the attribute is a numeric type.
7. (Original) The process of claim 3 wherein the attribute is a dimensionality.
8. (Original) The process of claim 1 wherein the ordered set is a linked list data structure.
9. (Previously Presented) The process of claim 8 wherein the linked list data structure is a tree data structure, the tree data structure including  $m + n$  nodes, wherein  $m$  represents a number of independent signals and  $n$  represents a number of composite signals.
10. (Canceled)

Application No.: 09/870,280

Docket No.: MWS-040RCE

11. (Original) The process of claim 1 further comprising:  
decomposing the first composite signal into the plurality of output signals in a demultiplexer.
12. (Original) The process of claim 1 further comprising viewing the ordered set contained in the first composite signal with a composite signal viewer.
13. (Original) The process of claim 1 wherein at least one of the input signal values is a second composite signal.
14. (Currently Amended) A computer implemented block diagram modeling process comprising:  
providing a first block and a second block, the blocks representing functional entities;  
generating a plurality of output signal values from the first and second block;  
grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and  
processing the composite signal in a third block; and  
storing the composite signal in a storage device.
15. (Original) The process of claim 14 wherein the ordered set is a linked list data structure.
16. (Previously Presented) The process of claim 14 wherein an input signal is a second composite signal.
17. (Previously Presented) The process of claim 14 further comprising decomposing the composite signal into a plurality of input signal values.
18. (Original) The process of claim 14 further comprising viewing the composite signal in a composite signal viewer.

Application No.: 09/870,280

Docket No.: MWS-040RCE

19. (Original) The process of claim 18 wherein the composite signal viewer displays the ordered set contained in the composite signal on a graphical user interface (GUI).
20. (Original) The process of claim 19 wherein the GUI is provided on an input/output device.
21. (Currently Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:
  - provide a plurality of blocks, each of the blocks representing functional entities;
  - generate a plurality of output signal values from the plurality of blocks;
  - group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; ~~and~~
  - output the first composite signal; and
  - store the first composite signal in a storage device.
22. (Original) The computer program product of claim 21 wherein the computer readable medium is a random access memory (RAM).
23. (Original) The computer program product of claim 21 wherein the computer readable medium is read only memory (ROM).
24. (Original) The computer program product of claim 21 wherein the computer readable medium is hard disk drive.
25. (Currently Amended) A processor and a memory configured to:
  - provide a plurality of blocks, each of the blocks representing functional entities;
  - generate a plurality of output signal values from the plurality of blocks;
  - group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; ~~and~~
  - output the first composite signal; and
  - store the first composite signal in a storage device.

Application No.: 09/870,280

Docket No.: MWS-040RCE

26. (Original) The processor and memory of claim 25 wherein the processor and the memory are incorporated into a personal computer.
27. (Original) The processor and memory of claim 25 wherein the processor and the memory are incorporated into a network server residing in the Internet.
28. (Original) The processor and memory of claim 25 wherein the processor and the memory are incorporated into a single board computer.
29. (Currently Amended) A computer implemented modeling process comprising:  
    providing a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signals;  
    grouping the output signals as an ordered set in a multiplexer as a composite signal; and  
    outputting the composite signal; and  
    storing the composite signal in a storage device.
30. (Original) The process of claim 29 wherein the ordered set is a tree data structure.
31. (Original) The process of claim 30 wherein the tree data structure is a linked list.
32. (Original) The process of claim 29 further comprising:  
    providing a composite signal viewer; and  
    viewing the ordered set in a graphical user interface executing in the composite signal viewer.
33. (Currently Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:  
    provide a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signal values;

Application No.: 09/870,280

Docket No.: MWS-040RCE

group the output signals as an ordered set in a multiplexer as a composite signal;  
and  
output the composite signal; and  
store the composite signal in a storage device.

34. (Currently Amended) A processor and memory configured to  
provide a plurality of blocks, each of the blocks representing a functional entity  
that generates one or more output signal values;  
group the output signals as an ordered set in a multiplexer as a composite signal;  
and  
output the composite signal; and  
store the composite signal in a storage device.

35. (Currently Amended) A method for providing a composite signal in a modeling  
environment, the method comprising the steps of:  
providing a plurality of output signals from one or more blocks;  
generating a composite signal comprising a set of the plurality of output signals; and  
providing the composite signal as an output signal; and  
storing the composite signal in a storage device.

36. (Currently Amended) A method for graphically representing a composite signal in a  
modeling environment, the method comprising the steps of :  
providing a plurality of output signals from one or more blocks, each output signal  
graphically indicated by a signal identifier; and  
providing a composite signal identifier to graphically indicate a grouping of signal  
identifiers, the composite signal identifier representing a composite signal comprising a set of  
the plurality of output signals; and  
storing the composite signal identifier in a storage device.